Bio-Data

1. **Name and full correspondence address:**

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3. **Research Areas:** Network-on-Chip Design and Test, Low Power Digital Testing, Thermal-Aware Testing, Fault Diagnosis

4. **Date of Birth:** 29th January, 1968
5. **Gender:** Male

6. **Academic Qualification**

Sl. No.	Degree	Year	Subject	University / Institution	% of marks / Grade Point
1.	Secondary	1983	General	WBBSE	78.4%
2.	Higher Secondary	1985	Science	WBCHSE	84.6%
1.	BE	1990	Computer Science and Technology	Calcutta University (B.E. College)	83.52%
2.	M.Tech	1992	Computer and Information Technology	Indian Institute of Technology, Kharagpur	9.58 (Out of 10)
3.	PhD	1996	Computer Science and Engineering	Indian Institute of Technology, Kharagpur	

7. **PhD Thesis:**

Title: Some Studies on Theory and Applications of Additive Cellular Automata
Guide: Prof. P. Pal Chaudhuri
Institute: Indian Institute of Technology Kharagpur
Year of Award: 1996

8. **Professional Recognition and Membership:**

Sl. No.	Name of Award	Awarding Agency	Year
1.	Senior Membership	IEEE, USA	2015
2.	Editorial Board Member	IET Circuits Devices and Systems	2013 onwards
3.	Best Engineering Faculty	Supreme	**********

9. Professional Experience:

Sl. No.	Positions Held	Name of the Institute	From	To
1.	Professor	Indian Institute of Technology Kharagpur	Aug 2011	Till date
2.	Associate Professor	Indian Institute of Technology Kharagpur	Dec 2004	Aug 2011
3.	Associate Professor	Indian Institute of Technology Guwahati	May 2002	Dec 2004
4.	Assistant Professor	Indian Institute of Technology Guwahati	Mar 2000	May 2002
5.	Network Manager	Indian Institute of Technology Kharagpur	Feb 1999	Mar 2000
6.	Lecturer	BE College (IIEST), Shibpur	July 1995	Feb 1999

10. Research Experience:

1) **Current h-index (as per Google Scholar citations):** 18
2) **No. of PhD Students Guided:** 10 (List attached)
3) **No. of Master's Thesis Guided:** 25
4) **Books published:** 5 (List attached)
5) **Peer reviewed international journal publications:** 53 (List attached)
6) **Peer reviewed international conference publications:** 69 (List attached)

11. Sponsored Projects:

- **Total Number:** 10
- **Major Sponsors:** DST, DeitY, MHRD, Synopsys Inc. etc.
- **Total Amount:** Rs. 204.09 Lakhs

12. Administrative Experience:

- Head, Dept. of Computer Science and Engineering, IIT Guwahati, March 2003 to September, 2004.
- Head, Computer Centre, IIT Guwahati, March 2003 to September, 2004.
- Warden, Nehru Hall of Residence, IIT Kharagpur, April 2008 to March 2010.
- Research Scholar's Coordinator, Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur.
- Master's Degree Coordinator, Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur.
- Member, Departmental Administrative Committee, Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur.
- Member, Departmental Academic Committee, Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur.

PhD Students Supervised (All at IIT Kharagpur)

Sl. No.	*Name*	*Thesis Title*	*Year of Award*	*Current Position*
1.	Chandan Giri	Test Infrastructure Design for Power Aware System-on-Chip Testing	2009	Assistant Professor, IIEST Shibpur
2.	Saurabh Chaudhury	Low Power Logic Optimization and Synthesis	2009	Associate Professor, NIT Silchar
3.	Sambhu Nath Pradhan	Genetic Algorithm based Logic Optimization and Synthesis Techniques with Area-Power Trade-Offs	2010	Associate Professor, NIT Agartala
4.	Santanu Kundu	Design and Evaluation of Mesh-of-Tree Network-on-Chip for Two- and Three-Dimensional Integrated Circuits	2011	LSI India R&D Pvt. Ltd. Bangalore
5.	Krishna Kumar S.	Power and Thermal-Aware Testing of Digital VLSI Circuits	2012	Professor. Federal Institute of Technology, Ernakulam
6.	Subhadip Kundu	Diagnosis Techniques for Identifying Faults in Digital VLSI System	2013	Engineer, Synopsys Bangalore
7.	Pradip Sahu	Application mapping strategies for Network-on-Chip topologies	2013	Professor, College of Engineering and Technology, Bhubaneswar
8.	Soumya J.	Application-Specific and Reconfigurable Network-on-Chip Design	2015	Assistant Professor, BITS Pilani, Hyderabad
9.	Tapas Maiti	Customizing Incompletely Specified Test Pattern Set for Power, Thermal and Confidence Aware Testing and Fault Diagnosis	2015	Associate Professor, College of Engineering and Management, Kolaghat
10.	Kanchan Manna	Thermal-Aware Design and Test Techniques for Two- and Three-Dimensional Networks-on-Chip	2016	Postdoctoral Fellow, University of Washington, USA

Sponsored Projects Handled as Principal Investigator

1. **Title:** Development of CAD tools for identification of logical equivalence of library elements, and identification of false paths in a switch level network.
   Amount: Rs. 1.17 Lakh
   Sponsor: Motorola India Electronics Ltd., Bangalore
   Duration: 1 year
   Brief summary: The objective of this project was to develop a set of CAD tools that would be useful to the practicing engineers of Motorola, for their physical design automation process. The project has been successfully completed.

2. **Title:** Campus-wide Electronic Payment System
   Amount: Rs. 10 Lakh
   Sponsor: Ministry of Human Resource Development, Govt. of India
   Duration: 2 years
   Brief summary: The objective of this project was to set up a laboratory to carry out E-commerce related teaching and research activities, and to pertain training to the people interested in this area. The project has been successfully completed.

3. **Title:** Designing a PC based integrated VLSI CAD tool for low power logic synthesis and testing (9.6)
   Amount: Rs. 9.6 Lakh
   Sponsor: Department of Science & Technology, Govt. of India
   Duration: 3 years
   Brief summary: The objective of this project was to design a set of CAD tools running on PC platform for low power logic synthesis. A number of tools have been designed for two-level and multi-level logic synthesis, FSM state encoding etc. Some initial work has also been done on low power testing of combinational circuits. The project has been successfully completed.

4. **Title:** Campus-wide Electronic Payment System (Modernization)
   Amount: Rs. 5 Lakh
   Sponsor: Ministry of Human Resource Development, Govt. of India
   Duration: 2 years
   Brief summary: The objective of this project was to modernize the laboratory set up earlier to carry out E-commerce related teaching and research activities, and to pertain training to the people interested in this area. The project has been successfully completed.

5. **Title:** Efficient testing for system-on-chip design – a new VLSI manufacturing paradigm
   Amount: Rs. 9.4 Lakh
   Sponsor: Department of Science & Technology, Govt. of India
   Duration: 3 years
   Brief summary: The objective of the project was to come up with testing strategies for System-on-Chip designs. It includes designing efficient test access mechanism, test scheduling, test data compression, and low power testing of SoCs. The project has been completed successfully.

6. **Title:** Power-aware Mesh-of-Tree based Network-on-Chip Design and Test
   Amount: Rs. 17.93 Lakh
   Sponsor: Department of Science & Technology, Govt. of India
   Duration: 3 years
   Brief summary: The objective of the project was to perform power analysis of the NoC fabric and study the power-performance behaviour, low power router design, perform voltage

and frequency scaling, designing testing scheme for a class of NoC. The project has been completed successfully.

7. **Title:** Strategies for power reduction during VLSI circuit testing
   Amount: Rs. 54.05 Lakh
   Sponsor: Department of Information Technology, Govt. of India
   Duration: 3 years + 1 year extension
   Brief summary: In this project, a set of CAD tools have been designed for low power internal, external and memory testing for VLSI circuits and systems. The project has been successfully completed.

8. **Title:** Strategies for thermal-aware Network-on-Chip design
   Amount: Rs. 25.03 Lakh
   Sponsor: Department of Science and Technology, Govt. of India
   Duration: 3 years
   Brief summary: The project aims at developing techniques for mapping applications onto NoC fabric to achieve thermal aware design styles. So far, works have been completed for two-dimensional NoCs. Both exact and heuristic methods have been developed for the same. The project has been completed successfully.

9. **Title:** Thermal-aware testing of VLSI circuits and systems
   Amount: Rs. 49.91 Lakh
   Sponsor: Department of Information Technology, Govt. of India
   Duration: 3 years
   Brief summary: The objective of this project has been to develop a set of CAD tools for thermal-aware testing. Techniques have been developed for test pattern customization, reordering, scan chain design at circuit level. At system level, it has addressed the issues of thermal-aware SoC and NoC testing. Some initial works have also been carried out for 3D ICs.

10. **Title:** Fault diagnosis techniques for yield enhancements
    Amount: Rs. 22 Lakh
    Sponsor: Synopsys Inc., USA
    Duration: 1 year
    Brief summary: The project aims at diagnosing faults that might have occurred in a chip that has failed a manufacturing test. The failed and passed patterns along with their responses are analyzed to identify a set of probable faults in the circuit. We aim at detection of multiple faults in the circuit with a very high degree of confidence. It also proposes to enhance the test pattern generator to better diagnose the faults. Circuit design for diagnosability is also a part of the project.

Publications

Text and Reference Books

[1] Compiler Design *by* S. Chattopadhyay (PHI Learning Pvt. Ltd., 2005)
[2] System Software *by* S. Chattopadhyay (PHI Learning Pvt. Ltd., 2007)
[3] Embedded System Design (Second Edition) *by* S. Chattopadhyay (PHI Learning Pvt. Ltd., 2013)
[4] Network-on-Chip The Next Generation System-on-Chip Integration *by* S. Kundu, S. Chattopadhyay (CRC Press Taylor & Francis Group, 2014)
[5] Additive Cellular Automata: Theory and Applications (Volume I) *by* P. Pal Chaudhuri, D. Roy Chowdhury, S. Nandi, S. Chattopadhyay (IEEE Computer Society Press, 1997)

Journal Publications

[1] Temperature and Data Size Trade-off In Dictionary Based Test Data Compression by R. Karmakar, S. Chattopadhyay *Integration, the VLSI Journal*, Accepted(0)
[2] Integrated Through Silicon Via Placement and Application Mapping for 3D Mesh Based NoC Design *by* K. Manna, S. Swami, S. Chattopadhyay, I. Sengupta *ACM Transactions on Embedded Computing Systems*, Accepted (0)
[3] In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers *by* B. Ghoshal, K. Manna, S. Chattopadhyay, I. Sengupta *IEEE Transactions on VLSI*, 24(1), pp. 393-397 (2016)
[4] Small Test Set Generation with High Diagnosability *by* A. Bhar, S. Chattopadhyay, I. Sengupta, R. Kapur *Journal of Circuits, Systems and Computers*, 25(4) (2016)
[5] Integrated Core Selection and Mapping for Mesh based Network-on-Chip Design with Irregular Core Sizes *by* Soumya J., K. Naveen Kumar, S. Chattopadhyay *Journal of Systems Architecture*, 61(9), 410-422 (2015)
[6] Window-Based Peak Power Model and Particle Swarm Optimization Guided 3-Dimensional Bin Packing for SoC Test Scheduling *by* R. Karmakar, S. Chattopadhyay *Integration, the VLSI Journal*, 50, pp. 61-73 (2015)
[7] Thermal-aware Multifrequency Network-on-Chip Testing using Particle Swarm Optimization *by* K. Manna, V.C. Reddy, S. Chattopadhyay, I. Sengupta *International Journal of High Performance Systems Architecture*, 5(3) (2015)
[8] Scan-chain Masking for Diagnosis of Multiple Chain Failures in a Space Compaction Environment *by* S. Kundu, S. Chattopadhyay, I. Sengupta, R. Kapur *IEEE Transactions on VLSI*, 23(7), pp. 1185-1195 (2015)
[9] Reconfigurable Data Parallel Constant Geometry FFT Architectures on Network-on-Chip *by* N. Prasad, S. Chattopadhyay, I. Chakrabarti *Microprocessors and Microsystems*, 39(8), 741-751 (2015)
[10] Integrated Mapping and Synthesis Techniques for Network-on-Chip Topologies with Express Channels *by* Sandeep DSouza, Soumya J, S. Chattopadhyay *ACM Transactions on Architecture and Code Optimization*, 12(4) (2015)
[11] Extending Kernighan-Lin Partitioning Heuristic for Application Mapping onto Network-on-Chip *by* P.K. Sahu, K. Manna, N. Shah, S. Chattopadhyay *Journal of Systems Architecture*, 60(7), pp. 562-578 (2014)
[12] Thermal Uniformity-Aware Application Mapping for Network-on-Chip Design *by* P.K. Sahu, K. Manna, T. Shah, S. Chattopadhyay *International Journal of Computer Applications*, 99(3), pp. 8-22 (2014)
[13] Area-Performance Trade-off in Floorplan Generation of Application-Specific Network-on-Chip with Soft Cores *by* Soumya J., S. Tiwary, S. Chattopadhyay *Journal of Systems Architecture*, 61(1), pp. 1-11 (2015)

[14] A Constructive Heuristic for Application Mapping onto Mesh based Network-on-Chip *by* P.K. Sahu, K. Manna, T. Shah, S. Chattopadhyay *Journal of Circuits, Systems, and Computers*, 24(8) (2015)
[15] Application-Specific Network-on-Chip Synthesis with Flexible Router Placement *by* Soumya J, S. Chattopadhyay *Journal of Systems Architecture*, 59, pp. 361-371 (2013)
[16] A Metric for Test Set Characterization and Customization Towards Fault Diagnosis *by* S. Kundu, S. Pal, S. Chattopadhyay, I. Sengupta, R. Kapur *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 32, pp. 1824-1828 (2013)
[17] Application Mapping Onto Mesh-Based Network-on-Chip Using Discrete Particle Swarm Optimization *by* P.K. Sahu, T. Shah, K. Manna, S. Chattopadhyay *IEEE Transactions on VLSI*, 22(2), pp. 300-312 (2014)
[18] Framework for Multiple-Fault Diagnosis Based on Multiple Fault Simulation Using Particle Swarm Optimization *by* S. Kundu, A. Jha, S. Chattopadhyay, I. Sengupta, R. Kapur *IEEE Transactions on VLSI*, 22(3), pp. 696-700 (2014)
[19] Multi-Application Network-on-Chip Design using Global Mapping and Local Reconfiguration *by* Soumya J, A. Sharma, S. Chattopadhyay *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 7(2), pp. 7.1-7.24 (2014)
[20] A Survey on Application Mapping Strategies for Network-on-Chip Design *by* P. K. Sahu and S. Chattopadhyay *Journal of Systems Architecture*, 59, pp. 60-76 (2013)
[21] Variable Ordering for Shared Binary Decision Diagrams targeting Node Count and Path Length Optimisation using Particle Swarm Optimization Technique *by* A. Mitra and S. Chattopadhyay *IET Computers and Digital Techniques*, 6, pp. 352-361 (2012)
[22] Design and Evaluation of Mesh-of-Tree based Network-on-Chip using Virtual Channel Router *by* S. Kundu, J. Soumya, S. Chattopadhyay *Microprocessors and Microsystems*, 36(6), pp. 471-488 (2012)
[23] An Efficient Routing Technique for Mesh-of-Tree based NoC and its Performance Comparison *by* K. Manna, S. Chattopadhyay, I. Sengupta *International Journal of High Performance Systems Architecture*, 4(1), pp. 25-37 (2012)
[24] Efficient Dont-Care Filling and Scan-Chain Masking for Low-Power Testing *by* S. Kundu, S. Chattopadhyay *International Journal of Computer Aided Engineering and Technology*, Vol. 4, 101-125 (2012)
[25] Multiplexer Based Multi-level Circuit Synthesis with Area-Power Trade-off *by* S.N. Pradhan, S. Chattopadhyay *Journal of Circuits, Systems, and Computers*, 21(5) (2012)
[26] Customizing Completely Specified Pattern Set Targeting Dynamic and Leakage Power Reduction During Testing *by* Krishna Kumar S., S. Kundu, S. Chattopadhyay *Integration, the VLSI Journal*, 45, 211-221 (2012)
[27] Low Power Finite State Machine Synthesis using Power-Gating *by* S.N. Pradhan, M. Tilak Kumar, S. Chattopadhyay *Integration, the VLSI Journal*, Vol. 44, pp. 175-184 (2011)
[28] AND-OR-XOR Network Synthesis with Area-Power Trade-off *by* S.N. Pradhan, M. Tilak Kumar, S. Chattopadhyay *Journal of Circuits, Systems, and Computers*, Vol. 20, 1019-1035 (2011)
[29] Power Aware Multi-level AND-XOR Network Synthesis *by* Ritesh Parikh, Santanu Chattopadhyay *International Journal of Computers and Applications*, 33(1) (2011)
[30] A New State Assignment Technique for Low Dynamic Power and Highly Testable FSM Synthesis *by* S. Chaudhury, J. S. Rao, S. Chattopadhyay *Journal of Low Power Electronics (JOLPE)*, 5(4), 464-473 (2009)
[31] Split Variable-Length Input Huffman Code (SVIHC) with Application to Test Data Compression for Embedded Cores in SOCs *by* C. Giri, B. M. Rao, S. Chattopadhyay *International Journal of Electronics*, 96(9), 935-942 (2009)
[32] Genetic algorithm-based FSM synthesis with area-power trade-offs *by* S. Chaudhury, K. T. Sistla, S. Chattopadhyay *Integration, the VLSI Journal*, 42, 376-384 (2009)
[33] Two-level AND-XOR Network Synthesis with Area-Power Trade-off *by* S.N. Pradhan, S. Chattopadhyay *International Journal of Computer Science and Network Security*, Vol-8, No. 9 (2008)

[34] Network-on-Chip Architecture Design Based On Mesh-of-Tree Deterministic Routing Topology *by* S. Kundu, S. Chattopadhyay *International Journal of High Performance Systems Architecture,* Vol. 1, No. 3 (2008)
[35] Fixed Polarity Reed-Muller Network Synthesis and its Application in AND-OR/XOR Based Circuit Realization with Area-Power Trade-off *by* S. Chaudhury, S. Chattopadhyay *IETE Journal of Research*, Vol. 54, No. 5 (2008)
[36] A Genetic Algorithm based Approach for System-on-Chip Test Scheduling using Dual Speed TAM with Power Constraint *by* C. Giri, D.K. Reddy Tipparthi, S. Chattopadhyay *WSEAS Transactions on Circuits and Systems*, 7, pp. 416-426 (2008)
[37] Circuit Partitioning for Mapping onto Dynamically Reconfigurable FPGAs *by* S. Chattopadhyay, P.S. Janakiraman *International Journal on Systemics, Cybernatics and Informatics*, pp. 77-81 (2008)
[38] System-on-Chip Test-time and Scan-power Minimization Integrating Core and Interconnect Testing *by* G. Das, S. Chattopadhyay, H. Bhaumik *International Journal on Computer Science and Network Security*, 9, pp. 201-209 (2009)
[39] Output phase assignment for area and power minimization in PLAs *by* S. Chaudhury, S. Chattopadhyay *Journal of the Indian Institute of Science*, 86, 33-43 (2006)
[40] Finite state machine decomposition for low power *by* S. Chattopadhyay. P.N.M Reddy *IETE Journal of Research*, 52, 35-43 (2006)
[41] Area Conscious State Assignment with Flip-Flop and Output Polarity Selection for Finite State Machine Synthesis - a Genetic Algorithm Approach *by* S. Chattopadhyay *The Computer Journal*, 48, pp. 443-450 (2005)
[42] Zero Aliasing Space Compaction with Cellular Automata *by* S. Chattopadhyay, Prashant *IETE Journal of Research*, 50 (2004) 425-431
[43] Finite State Machine State Assignment targeting Low Power Consumption *by* S. Chattopadhyay, P.N.M Reddy *IEE Proceedings - Computers and Digital Techniques*, 151, pp. 61-70 (2004)
[44] Partitioning Based Approach for Finite State Machine State Encoding Targeting Low Power *by* S. Chattopadhyay, P.N.M Reddy *IETE Journal of Research*, 49, pp. 379-385 (2003)
[45] Low Power State Assignment and Flipflop Selection for Finite State Machine Synthesis - A Genetic Algorithmic Approach *by* S. Chattopadhyay *IEE Proceedings - Computers and Digital Techniques*, 148, pp. 147-151 (2001)
[46] Theory and Application of Nongroup cellular automata for message authentificationT *by* P. Dasgupta, S. Chattopadhyay, I, Sengupta *Journal of Systems Architecture*, 47, pp. 383-404 (2001)
[47] Cellular Automata Based Recursive Pseudoexhaustive Test Pattern Generator *by* P. Dasgupta, S. Chattopadhyay, P. Pal Chaudhuri, I. Sengupta *IEEE Transactions on Computers*, 50, pp. 177-185 (2001)
[48] Highly Regular, Modular, and Cascadable Design of Cellular Automata based Pattern Classifier *by* S. Chattopadhyay, S. Adhikari, S. Sengupta, M. Pal *IEEE Transactions on VLSI Systems*, 8, pp. 724-735 (2000)
[49] Cellular Automata Array based Diagnosis of Board Level Faults *by* S. Chattopadhyay, D. Roy Chowdhuri, S. Bhattacharjee, P. Pal Chaudhuri *IEEE Transactions on Computers*, 47, pp. 817-828 (1998)
[50] KGPMIN: An Efficient Multi-level Multi-output AND-OR-XOR Minimizer *by* S. Chattopadhyay, S. Roy, P. Pal Chaudhuri *IEEE Transactions on Computer Aided Design*, 16, pp. 257-265 (1997)
[51] CAA Decoder for Cellular Automata based Byte Error Correcting Code *by* K. Sasidhar, S. Chattopadhyay, P. Pal Chaudhuri *IEEE Transactions on Computers*, 45, pp.1003-1016 (1996)
[52] Cellular Automata based Scheme for Solution of Boolean Equations *by* S. Bhattacharjee, S. Sinha, S. Chattopadhyay, P. Pal Chaudhuri *IEE Proceedings - Computers and Digital Techniques*, 143, pp. 174-180 (1996)

[53] Synthesis of Highly Testable Fixed-Polarity AND-XOR Canonical Networks - A Genetic Algorithm based Approach *by* S. Chattopadhyay, S. Roy, P. Pal Chaudhuri *IEEE Transactions on Computers*, 45, pp. 487-490 (1996)

[54] KGPMAP: a Library-based Technology-Mapping Technique for Antifuse based FPGAs *by* S. Chattopadhyay, S. Roy, P. Pal Chaudhuri *IEE Proceedings - Computers and Digital Techniques*, 141,pp. 361-368 (1994)

Conference Publications

[1] Thermal-Aware Preemptive Test Scheduling for Network-on-Chip Based 3D ICs *by* K. Manna, C.S. Sagar, S. Chattopadhyay, I. Sengupta *ISVLSI 2016*, pp. 529-534.

[2] Thermal-Aware Design and Test Techniques for Two-and Three-Dimensional Networks-on-Chip *by* K. Manna, S. Chattopadhyay, I. Sengupta *ISVLSI 2016*, pp. 583-586.

[3] Thermal-Safe Schedule Generation for System-on-Chip Testing *by* R. Karmakar, S. Chattopadhyay *VLSI Design 2016*, pp. 475-480.

[4] Optimization of the IEEE 1687 access network for hybrid access schedules *by* S. S. Nuthakki, R. Karmakar, S. Chattopadhyay, K. Chakrabarty *VTS 2016*, pp. 1-6.

[5] Test Infrastructure Development and Test Scheduling of 3D-Stacked ICs under Resource and Power Constraints *by* R. Karmakar, A. Agarwal, S. Chattopadhyay *ATS 2015*, pp. 73-78.

[6] An Integrated Approach for Improving Compression and Diagnostic Properties of Test Sets *by* S.S. Nuthakki, S. Chattopadhyay *ATS 2015*, pp. 151-156.

[7] Fault Tolerant Mesh Based Network-on-Chip Architecture *by* N. Chatterjee, S. Chattopadhyay *ISCAS 2015*, pp. 417-420.

[8] A Hardware Based Low Temperature Solution for VLSI Testing Using Decompressor Side Masking by A. Dutta, S. Kundu, S. Chattopadhyay. B. Das, ISACS 2015, pp. 637-640.

[9] Test Set Customization For Improved Fault Diagnosis Without Sacrificing Coverage *by* S.S. Nuthakki, S. Chattopadhyay, M. Chakraborty *ISCAS 2015*, pp. 1574-1577.

[10] TSV Placement and Core Mapping for 3D Mesh Based Network-on-Chip Design Using Extended Kernighan-Lin Partitioning *by* K. Manna, V.S.S. Teja, S. Chattopadhyay, I. Sengupta *ISVLSI 2015*, pp. 392-397.

[11] GA Based Diagnostic Test Pattern Generation For Transition Faults *by* A. Bhar, S. Chattopadhyay, I, Sengupta, R. Kapur *VDAT 2015*, pp. 1-6.

[12] Power- and Thermal-Aware Testing of VLSI Circuits and Systems *by* S. Chattopadhyay *VDAT 2015*, pp. 1.

[13] A Constructive Heuristic for Application Mapping onto an Express Channel based Network-on-Chip *by* S. D'Souza, Soumya J., S. Chattopadhyay *VDAT 2015*, pp. 1-6.

[14] Particle Swarm Optimization Approach for Low Temperature BIST by A. Dutta, S. Chattopadhyay *VDAT 2015*, pp. 1-6.

[15] Testing of 3D-Stacked ICs With Hard- and Soft-Dies - A Particle Swarm Optimization Based Approach *by* R. Karmakar, A. Agarwal, S. Chattopadhyay, *VDAT 2015*, pp. 1-6.

[16] A Spare Router Based Reliable Network-on-Chip Design *by* N. Chatterjee, S. Chattopadhyay, K. Manna *ISCAS 2014*, pp. 1957-1960.

[17] A Spare Link Based Reliable Network-on-Chip Design *by* N. Chatterjee, N. Prasad, S. Chattopadhyay *VDAT 2014*, pp. 1-6.

[18] A Locally Reconfigurable Network-on-Chip Architecture and Application Mapping Onto It *by* Soumya J., A. Sharma, S. Chattopadhyay *VDAT 2014*, pp. 1-6.

[19] Particle Swarm Optimization Guided Multi-frequency Power-aware System-on-Chip Test Scheduling Using Window-based Peak Power Model *by* R. Karmakar, A. Agarwal, S. Chattopadhyay *VDAT 2014*, pp. 1-6.
[20] Through Silicon Via Placement and Mapping Strategy for 3D Mesh Based Network-on-Chip by K. Manna, S. Chattopadhyay, I. Sengupta *VLSI-SoC 2014*, pp. 1-6.
[21] Techniques for Network-on-Chip (NoC) Design and Test *by* S. Chattopadhyay *VLSI Design 2014*, pp. 16-17.
[22] Thermal Aware Don't Care Filling to Reduce Peak Temperature and Thermal Variance during Testing *by* A. Dutta, S. Kundu, S. Chattopadhyay *ATS 2013*, pp. 25-30.
[23] An ATE Assisted DFD Technique For Volume Diagnosis of Scan Chains *by* S. Kundu, S. Chattopadhyay, I. Sengupta, R. Kapur *DAC 2013*, pp. 31:1 -31:6.
[24] Aggresive Scan Chain Masking For Improved Diagnosis of Multiple Scan Chain Failures *by* S. Kundu, S. Chattopadhyay, I. Sengupta, R. Kapur *ETS 2013*.
[25] Preemptive Test Scheduling for Network-on-Chip Using Particle Swarm Optimization *by* K. Manna, S. Singh, S. Chattopadhyay, I. Sengupta *VDAT 2013*, pp. 74-82.
[26] An Efficient Technique for Longest Prefix Matching in Network Routers *by* R. Govindaraj, I. Sengupta, S. Chattopadhyay *VDAT 2012*, pp. 317-326.
[27] Particle Swarm Optimization Based BIST Design for Memory Cores in Mesh Based Network-on-Chip *by* B. Ghoshal, S. Kundu, I. Sengupta, S. Chattopadhyay *VDAT 2012*, pp. 343-349.
[28] A Diagnosability Metric for Test Set Selection Targeting Better Fault Detection *by* S. Kundu, S. Chattopadhyay, I. Sengupta, R. Kapur *VLSI Design 2012*, pp. 436-441.
[29] Application Mapping onto Mesh Structured Network-on-Chip Using Particle Swarm Optimization *by* P.K. Sahu, P. Venkatesh, S. Gollapalli, S. Chattopadhyay *ISVLSI 2011*, pp. 335-336.
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